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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,414	11/04/2003	Richard Fastow	03-03	5776

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,414	FASTOW ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-11 and 13-18* is/are rejected.

7)☒ Claim(s) *3-5 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 re presented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-2,6-11,13-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hosono et al. (Pub. U.S. Patent No. 2003/0214853).

Regarding claim 1, Hosono et al. disclose a method for programming a group of at least one flash memory cell of an array (Figure 7), comprising:

A. performing a first pass of program verify and programming steps until each flash memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level (ABSTRACT, program verify control function) ; and

B. performing a second pass of program verify and programming steps until each flash memory cell of the group attains substantially the program verify level (ABSTRACT, erratic program verify control function).

Regarding claims 2, 6-9, 15-18, Hosono et al. disclose wherein the step A comprises a loop of the following steps: determining whether a flash memory cell of the group has not attained substantially X% of the program verify level, during the program verify step; and generating a programming pulse for the flash memory cell of the group that has not attained substantially X% of the program verify level, during the programming step (Figure 7, S3, S4, S5, [0007-0009]), and wherein (100%-X%) of the first program verify level is a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level (ABSTRACT, Figure 9), and wherein the at least one flash memory cell of the group is contained within a page of array (Figure 9, [0029]).

Regarding claims 10-11,13-14, Hosono et al. disclose a system for programming a group of at least one flash memory cell of an array (Figure 1) , comprising: means for performing a first pass of program verify and programming steps until each flash

memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level; and means for performing a second pass of program verify and programming steps until each flash memory cell of the group attains substantially the program verify level (ABSTRACT, Figure 7),and wherein the means for performing the first pass comprises: means for determining whether a flash memory cell of the group has not attained substantially X% of the program verify level, during the program verify step (S#, S4, S5); and means for generating a programming pulse (Figure 7, S3) for the flash memory cell of the group that has not attained substantially X% of the program verify level, during the programming step, and wherein the group includes a plurality of flash memory cells to be programmed to multi-level threshold voltages, the system further comprising: means for performing the first pass of program verify and programming steps until each flash memory cell of a first sub-group of the group attains a threshold voltage that is at least Y% of a first program verify level but less than the first program verify level, and until each flash memory cell of a second sub-group of the group attains a threshold voltage that is at least Z% of a second program verify level but less than the second program verify level; and means for performing the second pass of program verify and programming steps until each flash memory cell of the first sub-group attains substantially the first program verify level, and until each flash memory cell of the second sub-group attains substantially the second program verify level (Figures 9-12), and wherein (100%-Y%) of the first program verify level and (100%-Z%) of the second program verify level are each a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent

flash memory cells to a higher of the first and second program verify levels (ABSTRACT, Figure 9).

Allowable Subject Matter

5. Claim 3-5, 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-5, 12 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hosono et al. (Pub. U.S. Patent No. 20030214853), and others, does not teach the claimed invention having a method for programming a group of at least one flash memory cell of an array comprising a step having generating a programming pulse for flash memory cell of the group that has not attained the program verify level, during the programming step as claims 3, 12 disclose, and performing the second pass of program verify and programming steps until each flash memory cell of the first sub-group attains substantially the first program verify level, and until each flash memory cell of the second sub-group attains substantially the second program verify level as claim 4-5 disclose.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER